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(54) Abstract Title  
**Power factor correction circuit**

(57) A power factor correction circuit 10 comprises an series connection of a bridge rectifier, DB<sub>1</sub>, a first winding L<sub>a</sub>, a diode D<sub>1</sub> and an electrolytic capacitor C<sub>1</sub>; a series connection of the electrolytic capacitor C<sub>1</sub>, a second winding L<sub>b</sub> and a DC/DC converter 2; and a common core T<sub>r1</sub> wound round by the first winding L<sub>a</sub> and the second winding L<sub>b</sub>. The diode D<sub>1</sub> is able to switch between a reverse bias and a forward bias by controlling the polarities of the windings such that an input current always flows to the electrolytic capacitor C<sub>1</sub> during each sinusoidal period of an ac voltage. Also, a dc ripple voltage of the electrolytic capacitor C<sub>1</sub> will not rise due to a drop in load when the DC/DC converter 2 is operating in a continuous current mode. Furthermore an output of the DC/DC converter 2 will not be adversely affected by 120 Hz ac voltage input. The DC/DC converter may be a fly back converter (figure 9).

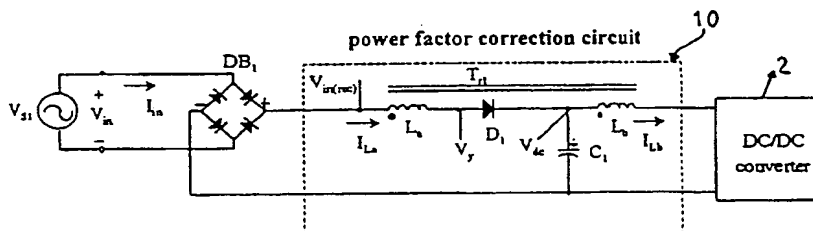


Fig8

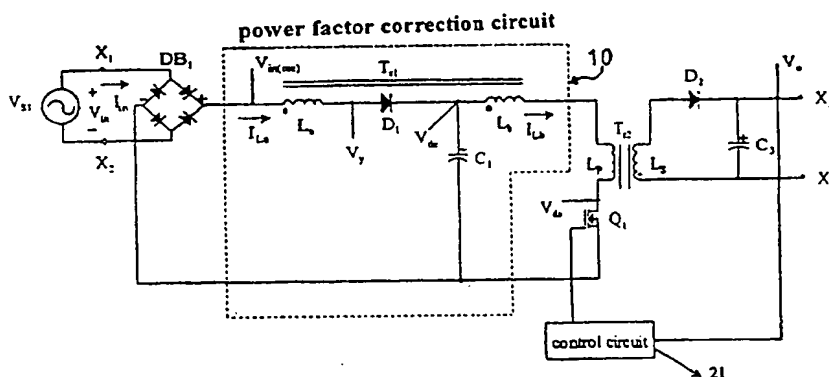


Fig9

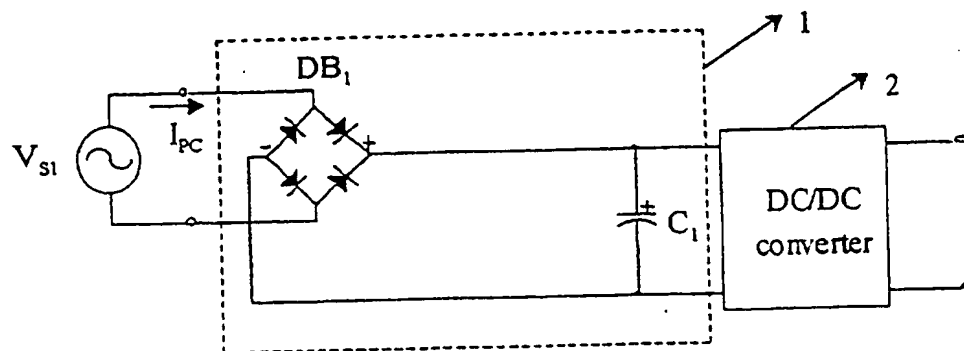


Fig1 (prior art)

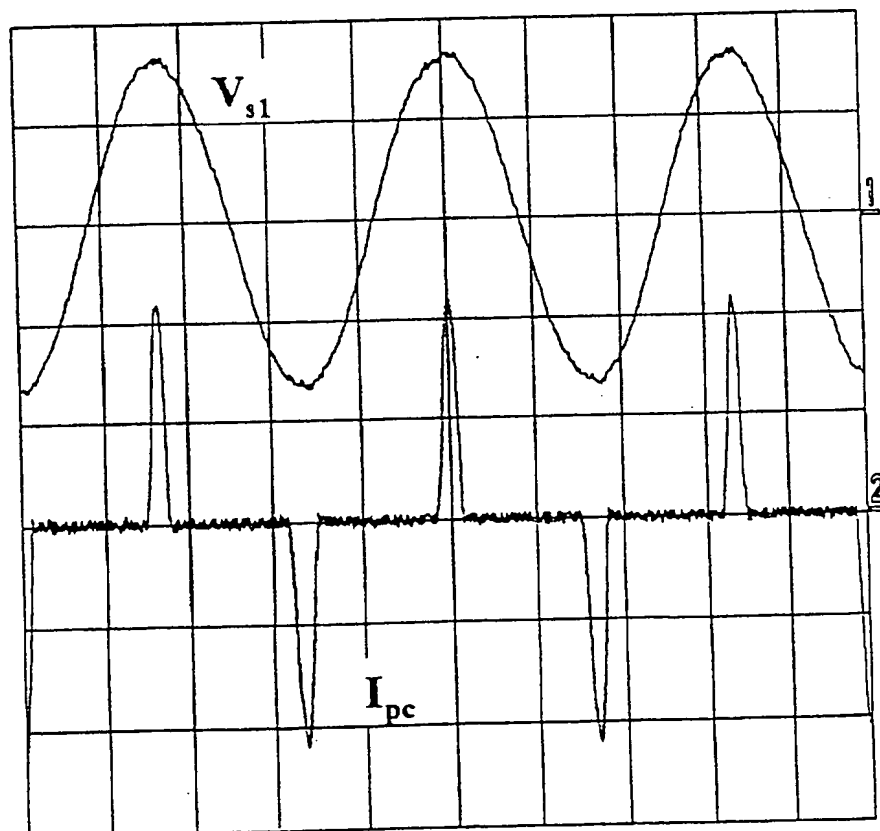


Fig2 (prior art)

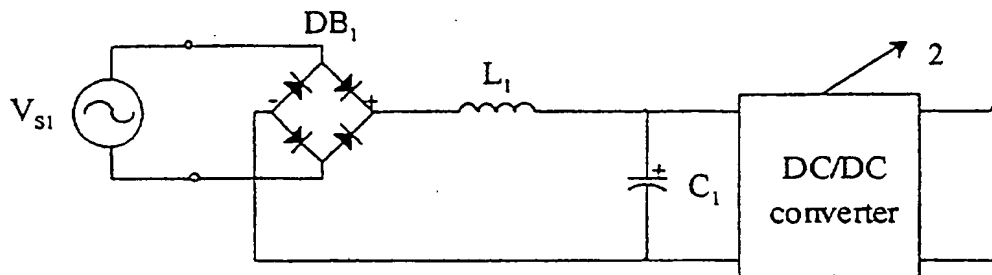


Fig3 (prior art)

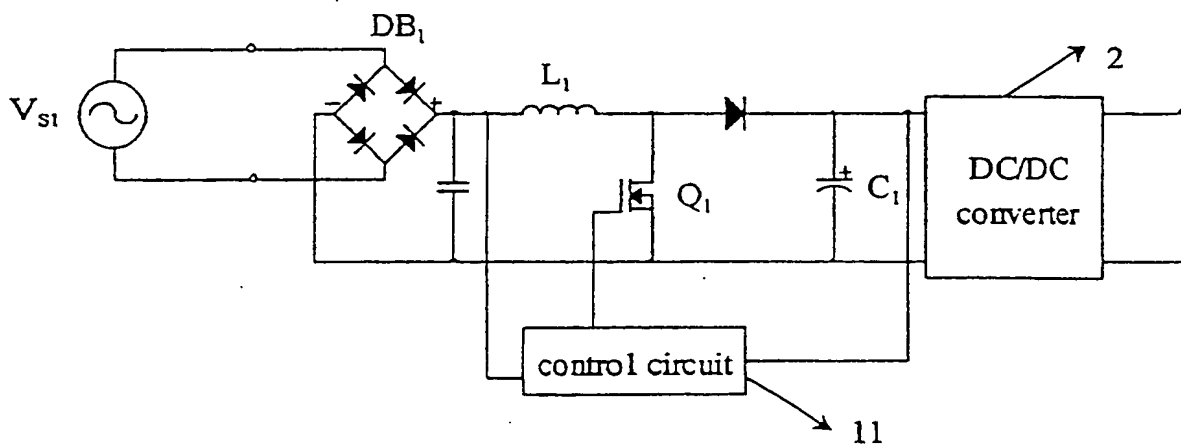


Fig4 (prior art)

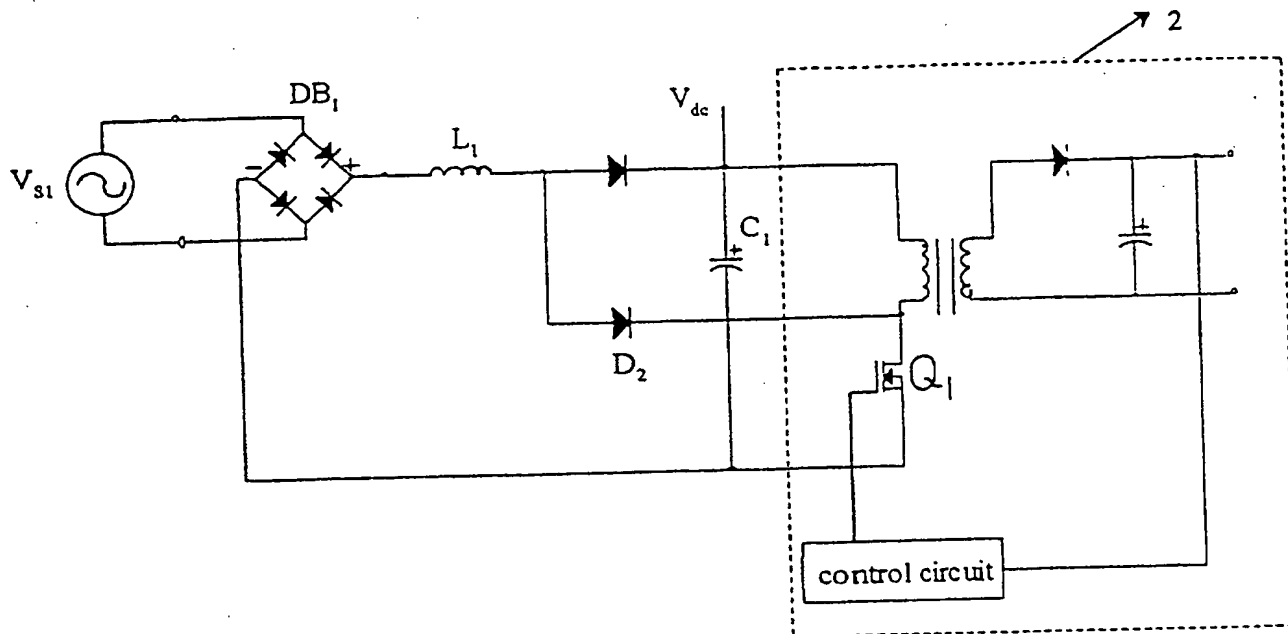


Fig5 (prior art)

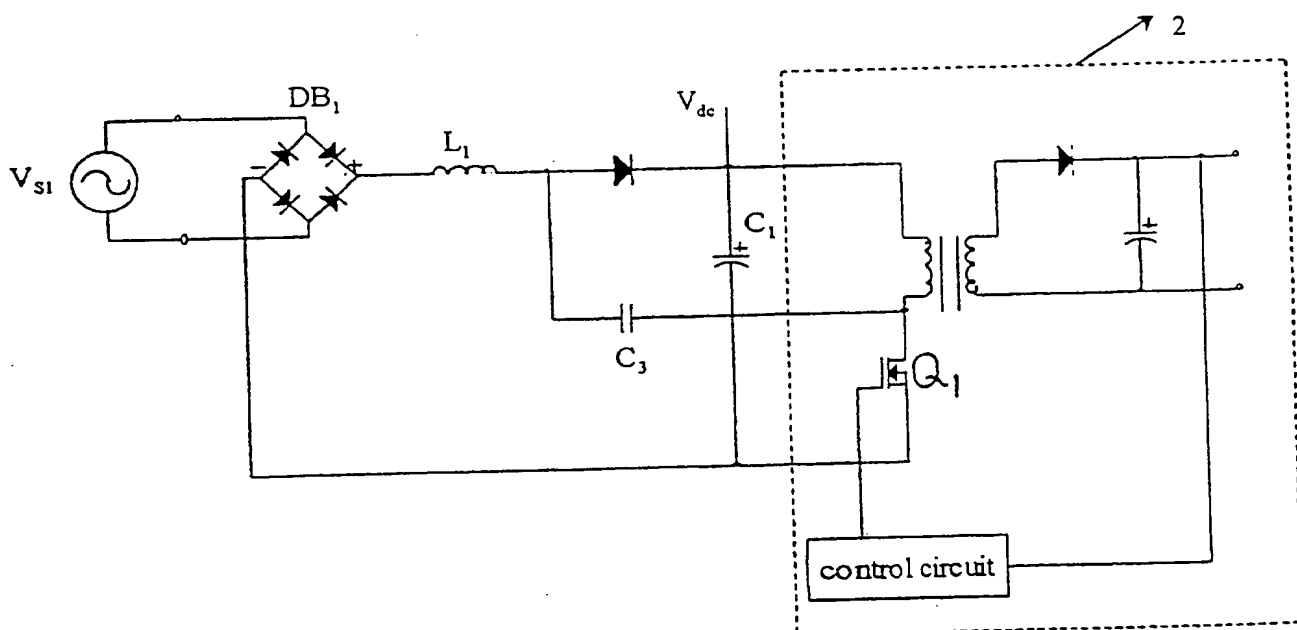


Fig6 (prior art)

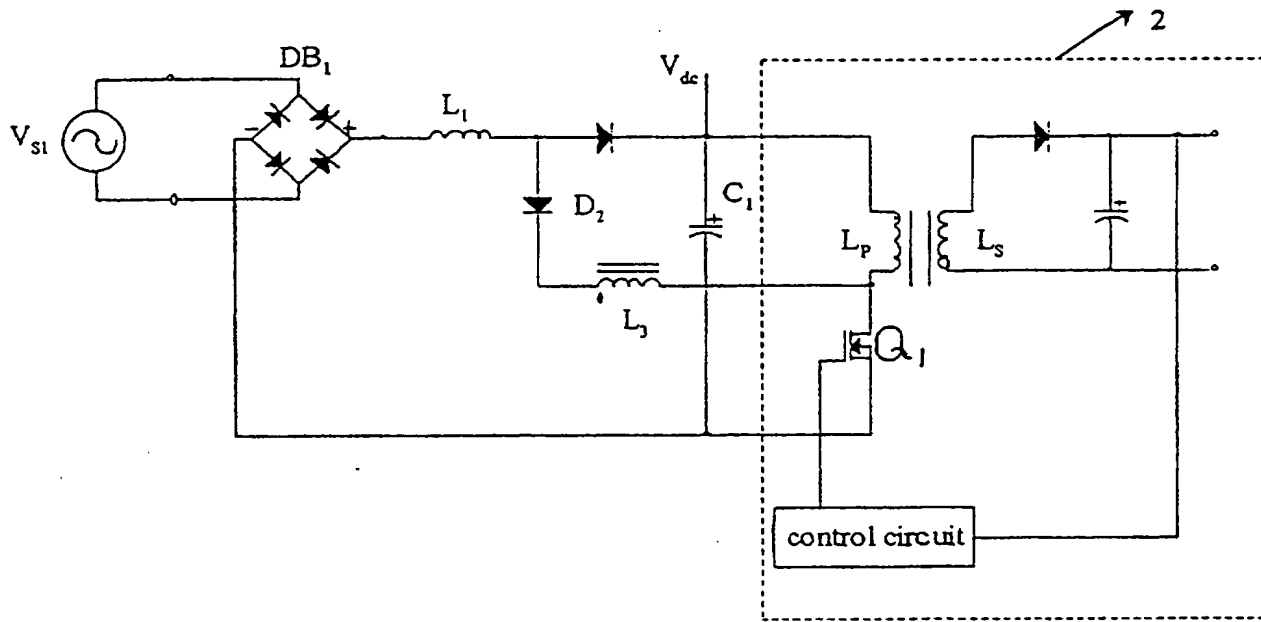


Fig7 (prior art)

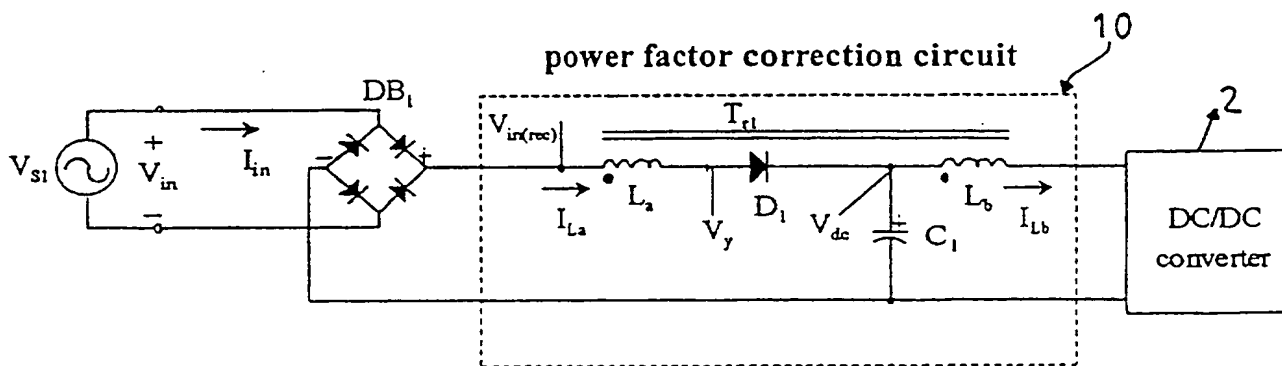


Fig8

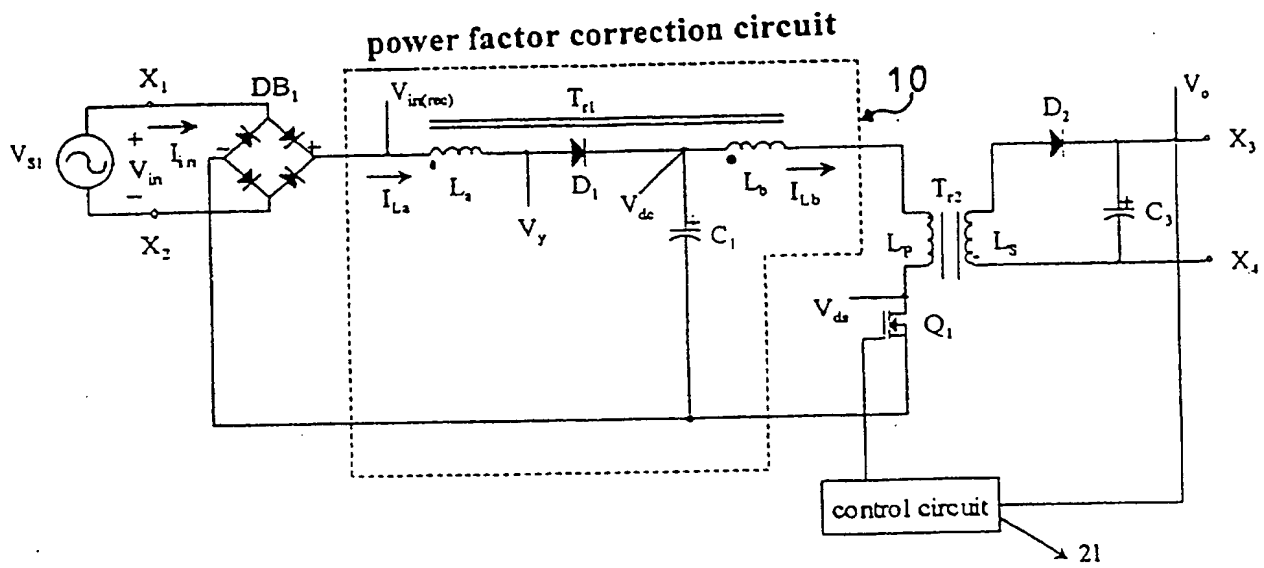


Fig9

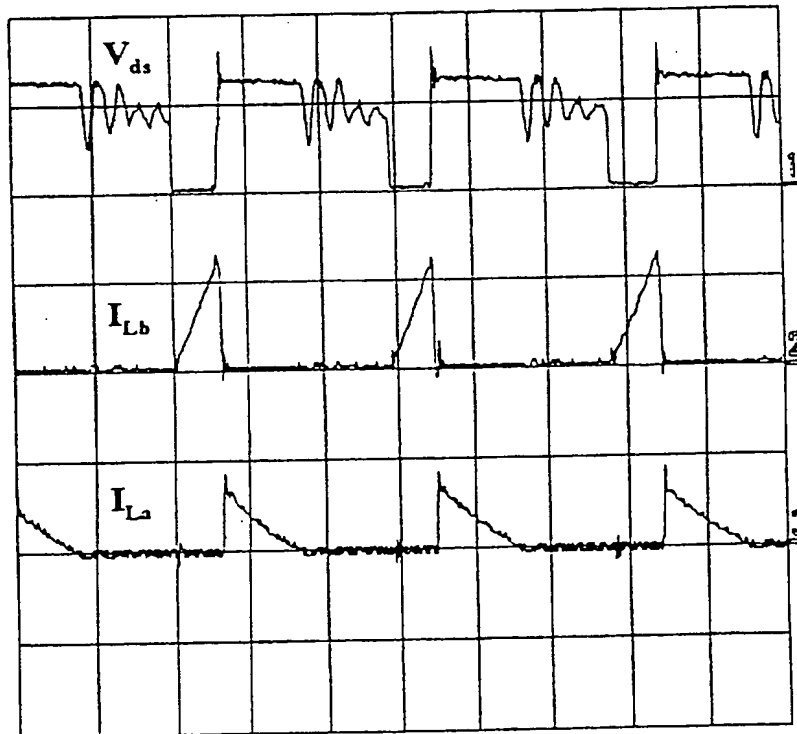


Fig10

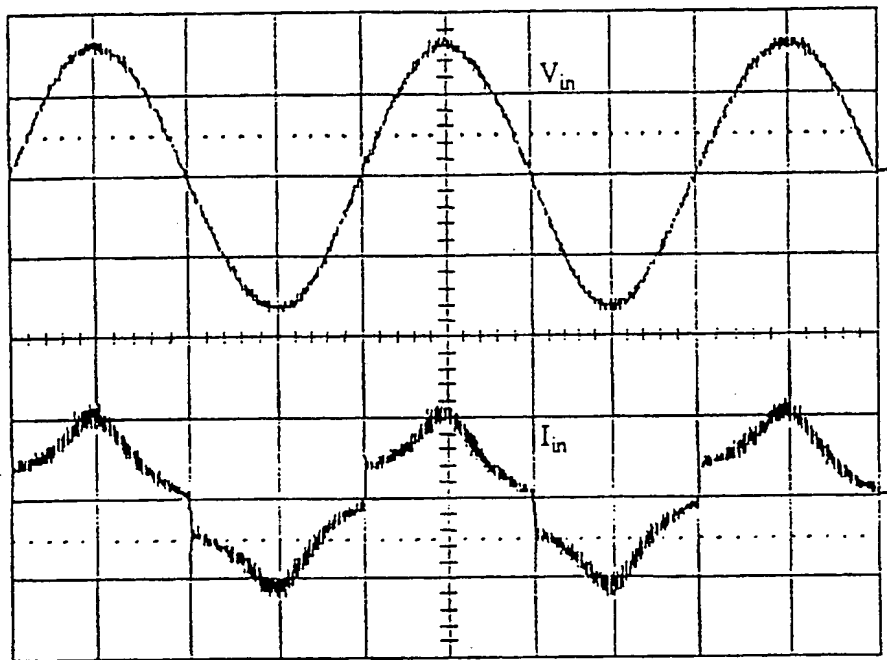


Fig11

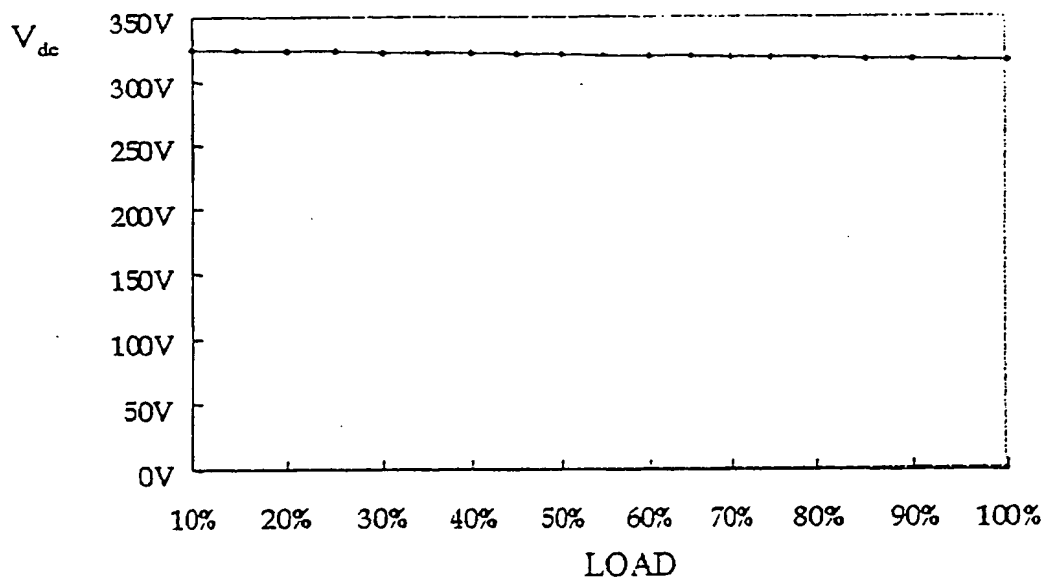


Fig12

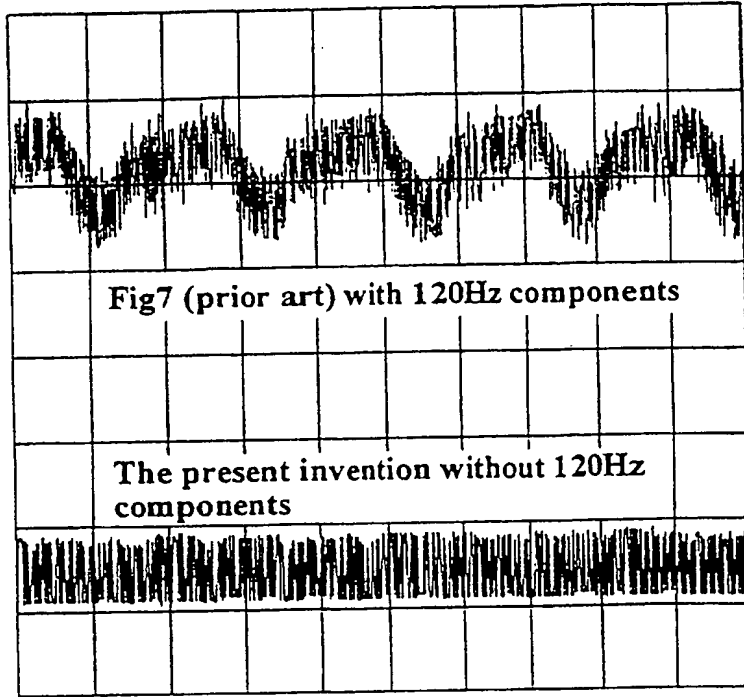


Fig13

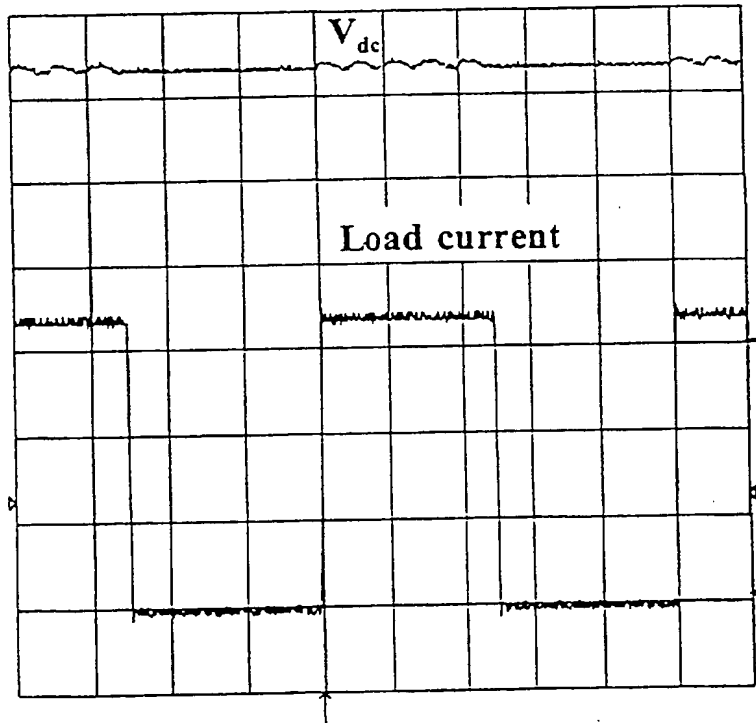


Fig14



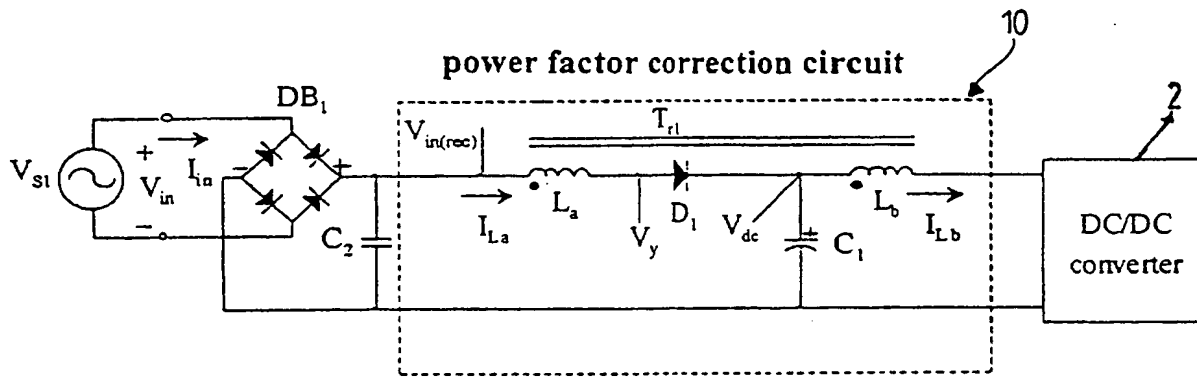


Fig15

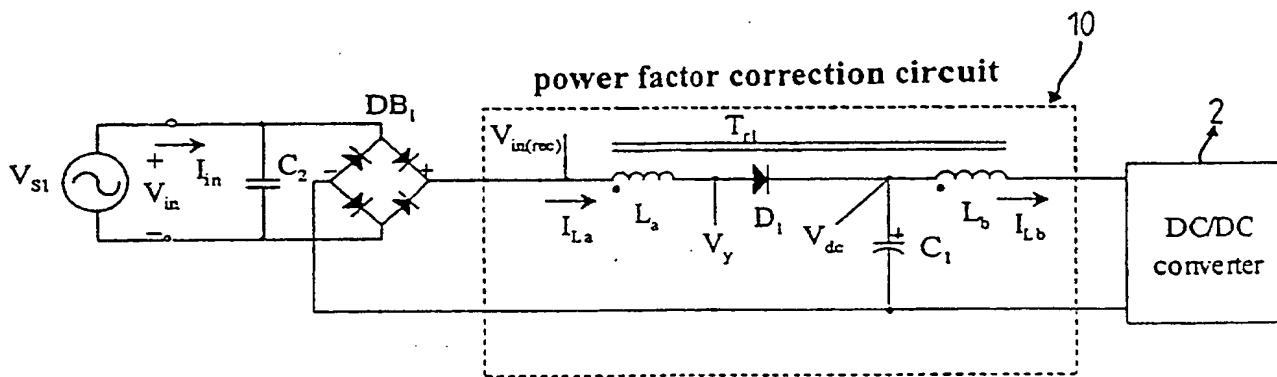


Fig16

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Table I

Input voltage: AC 230V/50Hz  
 Input power: 160W  
 PF: 0.977

CLASS A

Harmonic times	Current limit (A)	Measured current (mA)	comments
3	2.3	37.25	PASS
5	1.14	64.04	PASS
7	0.77	24.34	PASS
9	0.4	23.85	PASS
11	0.33	17.49	PASS
13	0.21	14.90	PASS
15	0.15	12.40	PASS
17	0.13	11.74	PASS
19	0.118	8.83	PASS
21	0.107	9.82	PASS
23	0.097	6.60	PASS
25	0.09	7.32	PASS
27	0.08	6.61	PASS
29	0.077	6.94	PASS
31	0.07	5.49	PASS
33	0.068	5.69	PASS
35	0.064	3.29	PASS
37	0.06	5.86	PASS
39	0.057	5.68	PASS

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**Table II**

Input voltage: AC 230V/50Hz  
Input power: 160W  
PF: 0.977

**CLASS D**

Harmonic times	Power ratio (ma/Watt)	Current limit (mA)	Measured current (mA)	comments
3	3.4	544.0	37.25	PASS
5	1.9	304.0	64.04	PASS
7	1	160.0	24.34	PASS
9	0.5	80.0	23.85	PASS
11	0.35	56.0	17.49	PASS
13	0.29	46.4	14.90	PASS
15	0.26	41.6	12.40	PASS
17	0.23	36.8	11.74	PASS
19	0.2	32.0	8.83	PASS
21	0.18	28.8	9.82	PASS
23	0.16	25.6	6.60	PASS
25	0.15	24.0	7.32	PASS
27	0.14	22.4	6.61	PASS
29	0.13	20.8	6.94	PASS
31	0.12	19.2	5.49	PASS
33	0.11	17.6	5.69	PASS
35	0.11	17.6	3.29	PASS
37	0.1	16.0	5.86	PASS
39	0.09	14.4	5.68	PASS

## POWER FACTOR CORRECTION CIRCUIT

The present invention relates to a power factor correction circuit for improving a power factor of an off-line switching power supply in order to comply with the requirements of Class A or Class D stipulated in harmonic current rules IEC-1000-3-2.

A typical off-line switching power supply is shown in FIG. 1. The supply comprises an AC/DC rectifier 1, and a DC/DC converter 2 in which an electrolytic capacitor  $C_1$  is connected as a filter for the bridge rectifier  $DB_1$ . As such, the electrolytic capacitor  $C_1$  begins to charge only when the bridge rectifier  $DB_1$  is conducted if the input ac voltage  $V_{s1}$  is higher than the voltage of the electrolytic capacitor  $C_1$ . Note that the input current  $I_{pc}$  is a pulsating current as shown in the graph of FIG. 2. The power factor of the input current of the conventional off-line switching power supply is significantly decreased (e.g., approximately 50%), and the total harmonics distortion (hereinafter referred as "THD") is even higher than 100% after the rectification performed by the AC/DC rectifier 1. As a result, the total harmonics is seriously distorted, the quality is poor, and, to the worse, the precious energy is wasted.

Thus, many countries have promulgated a number of harmonic current rules (e.g., IEC-1000-3-2) which specify the current waveshape of the power supply for manufacturers to obey in order to improve the efficiency and quality of the power source being supplied.

As such, various designs of power factor correction circuits have been proposed by researchers in order to improve power factor of the conventional off-line switching power supply. These designs have been located in a search as follows;

1. Inductor type power factor correction circuit:

As shown in FIG. 3, the prior art discloses a design in which a low frequency large winding  $L_1$  is in series between a bridge rectifier  $DB_1$  and a electrolytic capacitor  $C_1$ . The winding  $L_1$  and the capacitor  $C_1$  form a low pass filter to rectify the input current of a DC/DC converter 2. Such design is similar to the ballast for correcting the power factor of a fluorescent lamp in functionality. However, the winding  $L_1$  has the drawbacks for being relatively large, limited power factor improvement, and abnormal high temperature developed.

2. Active type power factor correction circuit:

As shown in FIG. 4, the prior art discloses a design in which the AC/DC rectifier is redesigned to form a two-stage circuit with the DC/DC converter 2. Further, a complex control circuit 11 and a large switch element  $Q_1$  are added therein to improve the power factor. However, it is relatively complex in circuit design and will cause high manufacturing cost.

3. Dither type power factor correction circuit of single-stage single-switch:

As shown in FIG. 5, the prior art is simple in circuit design. However, the whole circuit is redesigned, and a number of deficiencies have been found in use as follows:

a) The ripple voltage  $V_{dc}$  will rise to approximately 100% to 200% if the load suddenly drops significantly when the DC/DC converter 2 is operating in a continuous current mode. As such, a high-voltage electrolytic capacitor is required.

b) The alternating current component of the ac source  $V_{s1}$  will be brought

into the DC/DC converter 2 when the switch element  $Q_1$  is conducted. As a result, the output of the DC/DC converter 2 will be adversely affected by the 120 Hz ac voltage input, resulting in the rise of the ripple voltage.

c) The large winding  $L_1$  hardly improves the power factor when the DC/DC converter 2 is operating in the continuous current mode.

4. U.S. Pat. No. 5,301,095 to S. Teramoto is disclosed in FIG. 6. Teramoto's patent replaces the diode  $D_2$  of the dither type circuit shown in FIG. 5 with a small capacity capacitor  $C_3$  in order to improve the power factor. However, the deficiencies of b) and c) as stated above are not effectively eliminated.

5. U.S. Pat. No. 5,600,546 to Fu-Sheng Tsai is disclosed in FIG. 7. Tsai's patent adds another winding  $L_3$ , which is in series with the diode  $D_2$ , into the dither type circuit shown in FIG. 5. Such design will resolve the problem of the rise of ripple voltage  $V_{dc}$  of the electrolytic capacitor  $C_1$ , when the DC/DC converter 2 is operating in continuous current mode, by lowering the induction ratio  $L_p/L_1$  of the primary winding  $L_p$  of the DC/DC converter 2 to the winding  $L_1$ , or increasing the induction ratio  $L_3/L_p$  of the winding  $L_3$  to the winding  $L_p$ . However, the deficiencies of a) and c) as stated above are not effectively eliminated.

Thus, it is desirable to provide a power factor correction circuit in order to overcome the above drawbacks of prior art.

It is an object of the present invention to provide a power factor correction circuit comprising a series connection of a bridge rectifier, a first winding, a diode, and an electrolytic capacitor; a series connection of the electrolytic capacitor, a second winding, and a DC/DC converter; and a common core wound round by the first winding and the second winding. The diode is able to switch between a

reverse bias and a forward bias by controlling the polarities of the windings such that an input current always flows to the electrolytic capacitor during each sinusoidal period of an ac voltage. Further, the power factor of the off-line switching power supply is increased to above 0.9 by appropriately adjusting the induction ratio of the first winding to the second winding in order to comply with the requirements of Class A or Class D stipulated in harmonic current rules IEC-1000-3-2. Furthermore, the ripple voltage of the electrolytic capacitor will not rise if the load suddenly drops significantly when the DC/DC converter is operating in a continuous current mode. As such, the output of the DC/DC converter will not be adversely affected by the 120 Hz ac voltage input.

The invention will now be described further by way of example with reference to the accompanying drawings in which:-

FIG. 1 is a circuit diagram of a prior art off-line switching power supply;

FIG. 2 is a graph showing the wave shapes of the input voltage versus the input current of FIG. 1;

FIG. 3 is a circuit diagram of an inductor type power factor correction circuit;

FIG. 4 is a circuit diagram of an active type power factor correction circuit;

FIG. 5 is a circuit diagram of a dither type power factor correction circuit of single-stage single-switch;

FIG. 6 is a circuit diagram of U.S. Pat. No. 5,301,095;

FIG. 7 is a circuit diagram of U.S. Pat. No. 5,600,546;

FIG. 8 is a circuit diagram of a preferred embodiment of the present invention;

FIG. 9 is a modified circuit diagram of FIG. 8 in which the DC/DC converter

is a fly-back converter;

FIG. 10 is a graph showing the wave shapes of the voltage  $V_{ds}$  of the switch element versus the current  $I_{La}$ ,  $I_{Lb}$  of windings La, Lb of FIG. 9;

FIG. 11 is a graph showing the wave shapes of the input voltage  $V_{in}$  versus the input current  $I_{in}$  of FIG. 9;

FIG. 12 is a graph showing the voltage  $V_{dc}$  of the electrolytic capacitor  $C_1$  of FIG. 9 versus varying load;

FIG. 13 is a graph showing the wave shapes of the ripple voltages in the secondary electrolytic capacitors of the present invention shown in Fig. 9 and the prior art shown in FIG. 7;

FIG. 14 is a graph showing the dc ripple voltage  $V_{dc}$  of FIG. 9 versus varying load current;

FIG. 15 is a circuit diagram of a second embodiment of the present invention; and

FIG. 16 is a circuit diagram of a third embodiment of the present invention.

TABLE 1 is the experiment data of the harmonics of the input current  $I_{in}$  of the embodiment shown in Fig.9 comparing with the requirements of Class A stipulated in harmonic current rules IEC-1000-3-2; and

TABLE 1 is the experiment data of the harmonics of the input current  $I_{in}$  of the embodiment shown in Fig.9 comparing with the requirements of Class D stipulated in harmonic current rules IEC-1000-3-2.

Referring to FIG. 8, there is shown a preferred embodiment of a power factor correction circuit 10 constructed in accordance with the present invention. The power factor correction circuit 10 comprises a series connection of a bridge rectifier  $DB_1$ , a first winding  $L_a$ , a diode  $D_1$ , and an electrolytic capacitor  $C_1$ ; a



series connection of the electrolytic capacitor  $C_1$ , a second winding  $L_b$ , and a DC/DC converter 2; and a common core  $T_{r1}$  wound round by the first winding  $L_a$  and the second winding  $L_b$ .

In FIG. 9, the DC/DC converter 2 can be a fly-back converter comprising a transformer  $T_{r2}$ , a switch element  $Q_1$ , a control circuit 21, a diode  $D_2$  on a secondary side of the transformer  $T_{r2}$ , and a capacitor  $C_3$  on the secondary side of the transformer  $T_{r2}$ . The diode  $D_2$  and the capacitor  $C_3$  form an output filter. As to the transformer  $T_{r2}$ , ratio of the primary winding  $L_p$  to the secondary winding  $L_s$  with respect to the number of turns is  $N_p/N_s$ . A series connection consists of the primary winding  $L_p$ , the switch element  $Q_1$ , the electrolytic capacitor  $C_1$ , and the winding  $L_b$ . Another series connection consists of the secondary winding  $L_s$ , the diode  $D_2$ , and the capacitor  $C_3$ . An output voltage  $V_o$  is measured across the output terminals  $X_3$  and  $X_4$  by the control circuit 21 so as to generate a control signal for adjusting the conduction time of the switch element  $Q_1$ . As a result, the voltage  $V_o$  is kept at a predetermined value.

Again referring to Fig. 9, wherein  $V_{s1}$  is the ac input;  $V_{in}$  is an input voltage of the bridge rectifier  $DB_1$  measured across the input terminals  $X_1$  and  $X_2$ ;  $I_{in}$  is an input current thereof;  $V_{in(rec)}$  is an output voltage of the bridge rectifier  $DB_1$ ;  $I_{La}$  and  $I_{Lb}$  are currents of the first winding  $L_a$  and the second winding  $L_b$  respectively;  $V_y$  is a voltage measured between the first winding  $L_a$  and the diode  $D_1$ ; and  $V_{dc}$  is an input dc voltage of the electrolytic capacitor  $C_1$ .

In the above embodiment, the current  $I_{Lb}$  having a slope  $V_{dc}/(L_b+L_p)$  is generated on the secondary winding  $L_p$  when the switch element  $Q_1$  is conducted. Then, the current  $I_{Lb}$  flows from the anode of the electrolytic capacitor  $C_1$  through the windings  $L_b$ ,  $L_p$  and the switch element  $Q_1$  to the cathode of the electrolytic capacitor  $C_1$ . Since the windings  $L_b$ ,  $L_p$  wind round the same core  $T_{r1}$ , the polarity between the windings  $L_b$ ,  $L_p$  will then let the diode  $D_1$  be reverse

biased and act as an open circuit to block the current  $I_{La}$  of the winding  $L_a$ , i.e., the current  $I_{La}$  is approximately zero. The magnetic lines in the core  $T_{r1}$  will expand because the current  $I_{Lb}$  is still flowing through the winding  $L_b$ .

The magnetic lines in the core  $T_{r1}$  will diminish when the switch element  $Q_1$  is cut off. As a result, the polarity is reversed. Then the diode  $D_1$  is forward biased and acts as a closed circuit to conduct the current  $I_{La}$  of the winding  $L_a$  having a slope of  $(V_{in(rec)} - V_{dc})/L_a$  which flows from the bridge rectifier  $DB_1$  to the electrolytic capacitor  $C_1$ .

In FIG. 10, a graph shows the wave shapes of the voltage  $V_{ds}$  of the switch element  $Q_1$  versus the current  $I_{La}$  of the winding  $L_a$  and the current  $I_{Lb}$  of the winding  $L_b$ . In FIG. 11, a graph shows the wave shapes of the input voltage  $V_{in}$  versus the input current  $I_{in}$ . In view of these two graphs, it is found that the input current  $I_{in}$  generated in the present embodiment complies with the requirements of Class A or Class D stipulated in harmonic current rules IEC-1000-3-2. The above feature will be more apparent from table I and table II by comparing the experiment data of the harmonics of the input current  $I_{in}$  of the embodiment shown in Fig.9 with the requirements of Class D stipulated in harmonic current rules IEC-1000-3-2.

In view of the above, the power factor correction circuit 10 according to the present invention will make sure the input current  $I_{in}$  always flows to the electrolytic capacitor  $C_1$  during each sinusoidal period (i.e., the period of the switch element  $Q_1$  switching from conduction to cutoff and vice versa) of an ac voltage  $V_{in}$ . The power factor is then increased to above 0.9 by appropriately adjusting the induction of the windings  $L_a$ ,  $L_b$  and the induction of the secondary winding  $L_p$  of the transformer  $T_{r2}$  of the DC/DC converter 2. Moreover, the THD is dropped to below 15%.

As shown in FIG. 12, the voltage of the electrolytic capacitor  $C_1$  is kept at a

stable range when load is varied. Further, as shown in FIG. 13, the ripple output voltage of the DC/DC converter 2 of the present embodiment is not affected by the 120 Hz ac voltage input, while that of the prior art power supply shown in FIG. 7 is adversely affected. Furthermore, as shown in FIG. 14, the dc ripple voltage  $V_{dc}$  of the electrolytic capacitor  $C_1$  will not rise if the load suddenly drops significantly when the DC/DC converter 2 is operating in the continuous current mode.

FIG. 15 illustrates a second embodiment of the present invention in which a high frequency filter capacitor  $C_2$  is added to be in a parallel connection with the power factor correction circuit 10 for filtering out the high frequency component of the circuit 10. As such, the output current of the bridge rectifier DB1 is smoothed by the action of the capacitor  $C_2$ .

FIG. 16 illustrates a third embodiment of the present invention in which a high frequency filter capacitor  $C_2$  is added to be in a parallel connection with the bridge rectifier DB<sub>1</sub> for filtering out the high frequency component of the circuit 10. As such, the input current  $I_{in}$  of the ac source  $V_{s1}$  is smoothed by the action of the capacitor  $C_2$ .

Note that the fly-back converter as implemented in the above embodiments being readily substituted with a forward converter, a half-bridge converter, a full-bridge converter, a push-pull converter, or a boost converter should also be deemed as falling within the scope of the present invention.

While the invention herein disclosed has been described by means of specific embodiments, numerous modifications and variations could be made thereto by those skilled in the art without departing from the scope of the invention set forth in the claims.

## CLAIMS

1. A power factor correction circuit comprising:

a first series connection of a bridge rectifier, a first winding, a diode, and an electrolytic capacitor;

a second series connection of the electrolytic capacitor, a second winding, and a DC/DC converter; and

a common core wound round by the first winding and the second winding;

wherein the diode is able to switch between a reverse bias and a forward bias by controlling polarities of the windings such that an input current of an alternating current voltage always flows to the electrolytic capacitor during each sinusoidal period of the alternating current voltage.

2. The power factor correction circuit of claim 1, wherein the DC/DC converter further comprising:

a transformer in which a first series connection consists of a primary winding of the transformer, a switch element on a primary side of the transformer, the electrolytic capacitor on the primary side of the transformer, and the second winding, and a second series connection consists of a secondary winding of the transformer, a diode on a secondary side of the transformer, and a capacitor on the secondary side of the transformer; and

a control circuit connected between the switch element and an output of the DC/DC converter for measuring an output voltage of the converter so as to generate a control signal for adjusting a conduction time of the switch element for keeping the output voltage at a predetermined value.

3. The power factor correction circuit of claim 1 or 2, wherein a first high frequency filter capacitor is connected in parallel with the power factor correction circuit for filtering out a high frequency component of the power factor correction

circuit for smoothing an output current of the bridge rectifier.

4. The power factor correction circuit of claim 1 or 2, wherein a second high frequency filter capacitor is connected in parallel with the bridge rectifier for filtering out a high frequency component of the power factor correction circuit for smoothing the input current of the alternating current voltage.

5. A power factor correction circuit substantially as herein described with reference to and as illustrated in Figures 8, 9, 15 and 16 of the accompanying drawings.



Application No: GB 9909759.4  
Claims searched: 1- 4

Examiner: Ruth Patterson  
Date of search: 25 October 1999

**Patents Act 1977**  
**Search Report under Section 17**

**Databases searched:**

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:  
UK Cl (Ed.Q): H2F (F14); H2H (HAB)  
Int Cl (Ed.6): H02M (1/00); H02J (3/16, 3/18)  
Other: EPOQUE (WPI, JAPIO, EPODOC)

**Documents considered to be relevant:**

Category	Identity of document and relevant passage	Relevant to claims
	NONE	

- |   |   |   |  |
|---|---|---|--|
| X | Document indicating lack of novelty or inventive step   | A | Document indicating technological background and/or state of the art   |
| Y | Document indicating lack of inventive step if combined with one or more other documents of same category. | P | Document published on or after the declared priority date but before the filing date of this invention.          |
|   |   | E | Patent document published on or after, but with priority date earlier than, the filing date of this application. |
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